Complexity of Random Operators in Circuits With Arbitrary Gates

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Abstract

We consider boolean circuits computing n-operators $f : \{0,1\}^n \to \{0,1\}^n$. As gates we allow *arbitrary* boolean functions; neither fanin nor fanout of gates is restricted. An operator is linear if it computes n linear forms, that is, computes a matrix-vector product $A\vec{x}$ over $GF(2)$. We prove the existence of: (i) n-operators requiring about n^2 wires in any circuit; (ii) linear n-operators requiring about $n^{1+1/d}/(\log n)^{d+1/d}$ wires in depth-d circuits, and (iii) linear n-operators requiring about $n^2/\log n$ wires in depth-2 circuits, if either all output gates or all gates on the middle layer are linear.

Key words: Computational complexity; Boolean circuits; Matrix rigidity; Random operators; Kolmogorov complexity; Lower bounds

1. Introduction and results

We consider general circuits computing boolean operators n-operators $f : \{0,1\}^n \longrightarrow \{0,1\}^n$. As gates we allow *arbitrary* boolean functions of their inputs; there is no restriction on their fanin or fanout. Thus, the phenomenon which causes complexity of such circuits is *information transfer* rather than *information processing* as in the case of single functions. Such a circuit is a directed acyclic graph with n input nodes $x_1, \ldots, x_n$ and n output nodes $y_1, \ldots, y_n$. Each non-input node computes some boolean function of its predecessors. A circuit computes f if, for all $i = 1, \ldots, n$ the boolean function computed at the ith output node y_i is the ith component f_i of the operator $f = (f_1, \ldots, f_n)$. The *depth* of a circuit is the largest number of wires in a path from an input to an output node.

The *size* of a circuit is the total number of wires in it. We will denote by $s_d(f)$ the smallest number of wires in a general circuit of depth at most d computing f. If there are no restrictions on the depth, the corresponding measure is denoted by $s(f)$. Note that $s(f) \le s_1(f) \le n^2$ holds for any n-operator, so quadratic lower bounds are the highest ones.

Circuits of depth 2 constitute the first non-trivial model. Interest in depth-2 circuits comes from the following important result of Valiant [16]: if in every depth-2 circuit, computing f with $r = O(n/\ln\ln n)$ gates on the middle layer, at least $n^{1+\Omega(1)}$ wires must enter output gates, then f cannot be computed by log-depth circuit over $\{\&, \vee, \neg\}$ of linear size. To prove a non-linear lower bound for log-depth circuits is an old and well known problem in circuit complexity.

Super-linear lower bounds $s_2(f) = \Omega(n \log^2 n)$ where proved using graph-theoretic arguments by analyzing some super-concentration properties of the circuit as a graph [5, 8, 9, 11, 10, 1, 12, 13, 14].

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Higher lower bounds of the form $s_2(f) = \Omega(n^{3/2})$ were proved using relatively simple information theoretical arguments [4, 6]. For larger depth d known lower bounds are only slightly non-linear. All these bounds, however, are on the *total* number of wires, so they still have no consequences for log-depth circuits.

In fact, in the class of general circuits, even the question about the complexity of a *random* operator remained unclear. In particular, it was unclear whether operators requiring a quadratic number of wires (even in depth 2) exist at all?

Note that a direct counting argument, as in the case of constant fanin circuits, does not work for general circuits: already for $d > n + \log n$, the number 2^{2^d} of possible boolean functions that may be assigned to a node of fanin d may be larger than the total number 2^{n2^n} of n-operators.

Our first result is an observation that this bad situation can be excluded by just turning the power of circuits against themselves to ensure that, in an optimal circuit, no gate can have fanin larger than n. This leads us to

Theorem 1. *For almost all n-operators f, $s(f) = \Omega(n^2)$.*

An important class of operators are *linear* ones. Each such operator computes n linear forms, that is, a matrix-vector product $f_A(\vec{x}) = A\vec{x}$ over $GF(2)$. In the class of *linear* circuits—where we only allow linear boolean functions (parities and their negations) as gates—easy counting shows that most such operators require $\Omega(n^2/\log n)$ wires. It is also known that $O(n^2/\log n)$ of wires is also sufficient to compute any linear operator, even with linear depth-2 circuits [15, 3, 2].

But what is we allow arbitrary (non-linear) boolean functions as gates—can we then compute linear operators f_A more efficiently? The largest known lower bound for an *explicit* linear operator f_A has the form $s_2(f_A) = \Omega(n \log n)$ [10]. This raises the following question: Do *linear* n-operators with $s(f_A) = \Omega(n^2/\log n)$ exist at all? This question remains open even for depth-2 circuits.

The next three theorems partially answer this question.

Theorem 2. *For every $d \geq 2$, there exist $n \times n$ $(0,1)$ matrices A with*

$$s_d(f_A) = \Omega\left(\frac{n^{1+1/d}}{(\log n)^{d+1/d}}\right).$$

For depth $d = 2$ the bound is about $n^{3/2-o(1)}$, but this is still much smaller than the known upper bound $s_2(f_A) = O(n^2/\log n)$, holding even for linear circuits. We are only able to achieve this upper bound under additional restriction that either all output gates of all gates on the middle layer must be linear functions.

By a *middle-linear* (resp., *output-linear*) circuit we will mean a depth-2 circuit whose all gates on the middle (resp., output) layer are linear boolean functions.

It turns out that the non-linearity of *middle* gates cannot help to compute linear operators by depth-2 circuits more efficiently, and hence, linear n-operators requiring about $n^2/\log n$ in such circuits exist.

Theorem 3. *Every output-linear circuit of size L computing a linear n-operator can be transformed to an equivalent linear depth-2 circuit of size $L + n$.*

The second case—when only gates on the middle layer are required to be linear—is more delicate. That such circuits *can* be more powerful than linear ones, was shown in [7]. Given a boolean $n \times n$ matrix A, say that a circuit *weakly computes* the operator $f_A(\vec{x}) = A\vec{x}$ if it correctly computes it on all n unit vectors $\vec{e}_1, \ldots, \vec{e}_n$. Note that, for *linear* circuits, this is no relaxation: such a circuit weakly computes f_A iff it correctly computes the f_A on all inputs. Hence, some linear operators cannot be weakly computed by *linear* depth-2 circuits using fewer than $\Omega(n^2/\log n)$ wires. It is however shown in [7] that the situation changes drastically if we allow *non-linear* gates: then *any* linear n-operator can be weakly computed using only $O(n \log n)$ wires.

Still, using Kolmogorov complexity arguments, we can prove

Theorem 4. *If middle gates are required to be linear, then linear n-operators f_A with $s_2(f_A) = \Omega(n^2/\log n)$ exist.*

2. Proof of Theorem 1

Let $\mu(L)$ be the number of different n-operators $f : \{0,1\}^n \to \{0,1\}^n$ computable by boolean circuits with at most L wires. Our goal is to upper bound this number in terms of n and L, and compare this bound with the total number 2^{n2^n} of n-operators.

Take an optimal circuit with $\ell \le L$ wires computing some n-operator; hence, $\ell \le n^2$. Then $\ell = \sum_{i=1}^m d_i$, where $d_1, \dots, d_m$ are the fanins of its gates. It is clear that we need $m \ge n$ gates, since we must have n input gates. On the other hand, $m \le \ell + n + 2 \le 2n^2$ gates are always enough since every non-input gate, besides two possible constant gates, must have nonzero fanin.

We now make use of the fact that the gates in our circuits may be *arbitrary* boolean functions: This allows us to assume that $d_i \le n$ for all i. Indeed, if $d_i > n$, then we can replace the ith gate by the boolean function computed at this gate and join it to all n input variables; when doing this, the total number of wires in the circuit can only decrease.

The number of sequences $d_1, \dots, d_m$ of fanins with $0 \le d_i \le n$ does not exceed $(n+1)^m$. For each such sequence and for each $i = 1, \dots, m$, there are at most $\binom{m}{d_i} \le m^{d_i}$ possibilities to chose the set of inputs for the ith node and at most $2^{2^{d_i}}$ possibilities to assign a boolean function to this node. Hence,

$$\mu(L) \le (n+1)^m \prod_{i=1}^m m^{d_i} \prod_{i=1}^m 2^{2^d_i} = (n+1)^m m^{\sum_{i=1}^m d_i} 2^{\sum_{i=1}^m 2^{d_i}} .$$

Since $\sum_{i=1}^m d_i \le L \le n^2$ and $m \le 2n^2$, this yields

$$\log_2 \mu(L) \le \sum_{i=1}^m 2^{d_i} + O(n^2 \log_2 n) .$$

We now observe that at most $n/2$ nodes can have fanin larger than $2L/n$, for otherwise we would have more than $(2L/n) \cdot (n/2) = L$ wires in total. Since $m \le 2n^2$ and since the fanin of each gate does not exceed n, we obtain that

$$\sum_{i=1}^m 2^{d_i} \le (m - n/2) 2^{2L/n} + (n/2) 2^n \le 2n^2 4^{L/n} + 2^{n-1} .$$

Hence,

$$\log_2 \mu(L) \le 2n^2 4^{L/n} + n2^{n-1} + O(n^2 \log_2 n) . \tag{1}$$

Since the total number of operators $f : \{0,1\}^n \to \{0,1\}^n$ is 2^{n2^n}, the smallest number L of wires sufficient to compute all of them must satisfy $\log_2 \mu(L) \ge n2^n$. By (1), this implies

$$2n^2 4^{L/n} \ge n2^{n-1} - O(n^2 \log_2 n) .$$

Dividing both sides by $2n^2$, we obtain that $4^{L/n} = \Omega(2^n/n)$, and hence, $L = \Omega(n^2)$. □

3. Proof of Theorem 2

We will prove the theorem for $d = 2$; the argument in the general case is the same. Recall that the *rigidity* $\mathscr{R}_A(r)$ of a $(0,1)$ matrix A over $GF(2)$ is the smallest number of entries of A that must be changed in order to reduce its rank over $GF(2)$ until r. That is,

$$\mathscr{R}_A(r) = \min\left\{|B| : \mathrm{rk}(A \oplus B) \leq r\right\},$$

where $|B|$ is the number of nonzero entries in B.

Take a depth-2 circuit $G = (V, E)$ computing $A\vec{x}$ and let L be the number of wires in it. Our goal is to prove that, for any $\alpha > 0$,

$$L \geq \frac{1}{\alpha}\sqrt{n \cdot \mathscr{R}_A\left(\frac{n}{\alpha}\right) - \frac{n^3}{\alpha}}\,. \tag{2}$$

Then we will make use of the fact that matrices of high rigidity exist.

The circuit has n input nodes $x_1, \ldots, x_n$ and n output nodes $y_1, \ldots, y_n$, the ith of which compute the scalar products $y_i = \langle \vec{a}_i, \vec{x} \rangle$ of input vector $\vec{x}$ with the ith row of A. For a node $v \in V$ let $d(v)$ be it fanin in the graph G.

Say that a node $v \in V$ is *large* if $d(v) > \alpha L/n$, and *small* otherwise. Note that the total number of large nodes in the circuit must be smaller than n/α, for otherwise we would have more than $(n/\alpha) \cdot (\alpha L/n) = L$ wires. To prove the desired lower bound on L, we now argue as follows.

Set all large outputs y_i to constant 0, and remove all wires incident to such inputs. The resulting circuit computes a linear operator $A'\vec{x}$ for an $n' \times n$ submatrix $A' \leq A$ of A obtained by setting to 0's all its entries in the $n' < n/\alpha$ rows corresponding to large outputs y_i of the original circuit. Hence

$$|A - A'| \leq \frac{n^2}{\alpha}\,.$$

Let W_{large} be the set of all large nodes on the middle layer; hence $|W_{\mathrm{large}}| < n/\alpha$.

Say that an output node y_i *can see* the jth input x_j if either there is a direct wire from x_j to y_i or there is a length-2 path from x_j to y_i going through a node $v \notin W_{\mathrm{large}}$.

Since $d(y_i) \leq \alpha L/n$ and since $d(w) \leq \alpha L/n$ for all $w \notin W_{\mathrm{large}}$, each output gate can see at most $(\alpha L/n)^2$ inputs. Let $B = (b_{ij})$ be the matrix obtained from $A' = (a_{ij})$ by setting $b_{ij} := 0$ if y_i can see x_j, and $b_{ij} := a_{ij}$ otherwise. Hence $B \leq A'$ and, by the previous observation,

$$|A' - B| \leq n(\alpha L/n)^2 = (\alpha L)^2/n\,. \tag{3}$$

We can now remove all wires leaving small gates on the middle layer (that is, gates outside W_{large}) and the obtained circuit still computes $B\vec{x}$. But this circuit has only $|W_{\mathrm{large}}| < n/\alpha$ nodes on the middle layer. If on two input vectors $\vec{x}$ and $\vec{y}$ the gates on these middle nodes compute the same values, then $B\vec{x} = B\vec{y}$. This implies that

$$\mathrm{rk}(B) \leq |W_{\mathrm{large}}| < \frac{n}{\alpha}\,.$$

The matrix B was obtained from our original matrix A by changing at most $|A - A'| + |A' - B| \leq n^2/\alpha + (\alpha L)^2/n$ entries, and this change has reduced the rank of A till $r < n/\alpha$. Hence

$$\mathscr{R}_A\left(\frac{n}{\alpha}\right) \leq \frac{n^2}{\alpha} + \frac{(\alpha L)^2}{n}$$

from which (2) follows.

The case of depth-d circuits for $d \geq 3$ the argument is almost the same. In this case we take W_{large} to be the set of all inner nodes (that is, nodes different from inputs and outputs) of fanin larger than $\alpha L/n$. The estimate (3) turns then to $|A' - B| \leq n(\alpha L/n)^d$. The rest is the same using this (worse) estimate, and yields the lower bound

$$s_d(f_A) \geq \frac{1}{\alpha^d} \sqrt[d]{n^{d-1} \cdot \mathcal{R}_A\left(\frac{n}{\alpha}\right) - \frac{n^{d+1}}{\alpha}}\,. \tag{4}$$

To obtain the lower bound stated in Theorem 2, we use the fact that matrices of high rigidity exist. Namely, using counting arguments, Valiant [16] has shown that $n \times n$ $(0,1)$ matrices A with $\mathcal{R}_A(r) = \Omega\left((n-r)^2/\log n\right)$ for all $r \leq n - O(\sqrt{n})$ exists. Taking $\alpha = \Theta(\log n)$ in (4) yields the desired lower bound on $s_d(f_A)$. $\square$

4. Proof of Theorem 3

Let A be an m-by-n $(0,1)$-matrix, and let F be a depth-2 circuit computing $A\vec{x}$. We may assume, for simplicity, that there are no direct wires from inputs to outputs: this can be easily achieved by adding n new wires.

Let $h = (h_1, \ldots, h_r)$ be the operator : $\{0,1\}^n \to \{0,1\}^r$ computed by the gates on the middle layer. Let also B be the m-by-r adjacency $(0,1)$-matrix of the bipartite graph formed by the wires joining the gates on the middle layer with those on the output layer.

Assume that all output gates of F are linear boolean functions. Then $A\vec{x} = B \cdot h(\vec{x})$ for all $\vec{x} \in \{0,1\}^n$. Write each vector $\vec{x} = (x_1, \ldots, x_n)$ as the linear combination $\vec{x} = \sum_{i=1}^n x_i \vec{e}_i$ of unit vectors $\vec{e}_1, \ldots, \vec{e}_n \in \{0,1\}^n$, and replace the operator H computed on the middle layer by a *linear* operator $h'(\vec{x}) := \sum_{i=1}^n x_i h(\vec{e}_i) \pmod 2$. Hence, $h'(\vec{x}) = \vec{x}^\top M$, where M is an $n \times r$ matrix with rows $h(\vec{e}_1), \ldots, h(\vec{e}_n)$. Using the linearity of the matrix-vector product, we obtain that (with all sums mod 2):

$$B \cdot h(\vec{x}) = A \cdot \left(\sum x_i \vec{e}_i\right) = \sum x_i A\vec{e}_i = \sum x_i B \cdot h(\vec{e}_i) = B \cdot h'(\vec{x})\,.$$

Hence, the new (linear) circuit F' computes $A\vec{x}$ as well. It remains to show that the number of wires in F' does not exceed the number of wires in F.

The wires on the second level haven't changed at all. To show that the *number* of wires on the first level has not increased as well, let fanout(x_i) be the fanout of the ith input node x_i, and fanin(h_j) the fanin of the jth gate h_j on the middle layer. Then $\sum_{i=1}^n \text{fanout}(x_i) = \sum_{j=1}^r \text{fanin}(h_j)$ is the total number L of wires on the first level. Since $A\vec{0} = \vec{0}$, we can assume that $h(\vec{0}) = \vec{0}$, that is, $h_j(\vec{0}) = 0$ for all $j = 1, \ldots, r$. Now we make a simple (but crucial) observation: if there is no wire from x_i to h_j, then $h_j(\vec{e}_i) = h_j(\vec{0}) = 0$. This implies that the jth column of M can have at most fanin(h_j) ones. Since the number of wires on the first level of F' is just the total number of 1's in M, we are done. $\square$

5. Proof of Theorem 4

We use Kolmogorov complexity argument. Let A be a boolean $n \times n$ matrix of Kolmogorov complexity $\Omega(n^2)$. Hence, the linear operator $f_A(\vec{x}) = A\vec{x}$ cannot be described using fewer than $\Omega(n^2)$ bits.

Fix an arbitrary depth-2 circuit F computing f_A, and assume that all its gates on the middle layer are linear. Let L be the number of wires in F. As in the previous section, we may assume that there are no direct wires from inputs to outputs. Our goal is to show that, using the circuit F, the operator f_A can be described using $O(L \log n)$ bits. This will imply the desired lower bound $L = \Omega(n^2/\log n)$ on the number of wires.

Let $v_1, \ldots, v_r$ nodes on the middle layer. Since at these nodes only linear functions are computed, the first level (between inputs and middle layer) computes some linear operator $\vec{y} = B\vec{x}$, where B is a boolean $r \times n$ matrix such that $B[i, j] = 0$ if there is no wire from input variable x_i to the node v_j.

Let C be an incidence $n \times r$ matrix of the second level of the circuit. Using these two matrices B and C as well as the fact that the operator computed by the circuit F is linear, we can encode the entire work of the circuit using $O(L \log n)$ bits as follows. Let L_1 be the number of wires on the first level (between input and middle layer), and L_2 be the number of wires on the second level (between the middle and output layers).

1. The matrix B can be described using $L_1\lceil \log_2 n\rceil$ bits. Indeed, if b_j denotes the number of 1's in the jh row of B, then $\sum_{j=1}^{r} b_j$ does not exceed the number L_1 of wires on the first level. Since the ith row of B can be described by $b_i\lceil \log_2 n\rceil$ bits, the entire matrix B can be described using $\sum_{j=1}^{r} b_j\lceil \log_2 n\rceil = L_1\lceil \log_2 n\rceil$ bits.
2. By the same argument, the matrix C can be described using $L_2\lceil \log_2 n\rceil$ bits.
3. For each output gate g_i, let B_i be the submatrix of B whose rows correspond to the d_i nodes on the middle layer seen by this gate. Let $\mathrm{Im}(B_i) = \{B_i\vec{x} \colon \vec{x} \in \{0,1\}^n\}$ be the column space of B_i. If this space has dimension t then any t linearly independent columns of B form its basis. Take the set $B_i' = \{\vec{u}_1, \ldots, \vec{u}_t\}$ of the first t linearly independent columns of B_i, and call it the *first basis* of $\mathrm{Im}(B_i)$.
4. Encode the behavior of g_i on this basis B_i' by a string of $t \le d_i$ bits $g_i(\vec{u}_1), \ldots, g_i(\vec{u}_t)$. The entire string, for all n output gates $g_1, \ldots, g_n$, has length at most $\sum_{i=1}^{n} d_i = L_2$.

Having this encoding, we can recover the value $g_i(\vec{x})$ of the ith output gate on a given input $\vec{x} \in \{0,1\}^n$ as follows.

1. Compute $\vec{y} = B_i\vec{x}$. We can do this since the ith row of C tells us what rows of B appear in B_i, and we know the entire matrix B.
2. Take the first basis B_i' of $\mathrm{Im}(B_i)$ and write $\vec{y}$ as a linear combination $\vec{y} = \sum_{k=1}^{t} \lambda_k \vec{u}_k$ of basis vectors.
3. Give $z_i = \sum_{k=1}^{t} \lambda_k g_i(\vec{u}_k)$ as an output. We can compute this number since we know the values $g_i(\vec{u}_1), \ldots, g_i(\vec{u}_t)$.

Since the circuit computes $A\vec{x}$, the ith output gate must compute the scalar product $\langle \vec{a}_i, \vec{x}\rangle$ of input vector $\vec{x}$ with the ith row $\vec{a}_i$ of A. Hence, $g_i(B\vec{x}) = \langle \vec{a}_i, \vec{x}\rangle$, meaning that g_i must be *linear* on $\mathrm{Im}(B)$, and hence, also on $\mathrm{Im}(B_i)$. Thus,

$$z_i = \sum_{k=1}^{t} \lambda_k g_i(\vec{u}_k) = g_i\left(\sum_{k=1}^{t} \lambda_k \vec{u}_k\right) = g_i(\vec{y}) = g_i(B_i\vec{x}) = g_i(B\vec{x}),$$

that is, z_i is a scalar product of $\vec{x}$ with the ith row of A, as desired. □

6. Conclusion

We have shown that linear operators requiring $\Omega(n^2/\log n)$ wires in any depth-2 circuit exits, if we require that all gates on the middle layer or all gates on the output layer must be linear. We conjecture, however, that this also holds without this requirement. An even more important question is to prove that some *explicit* linear operator requires $n^{1+\epsilon}$ wires in general depth-2 circuits. The highest known explicit lower bounds, even for linear circuits, have the form $\Omega(n \ln^{3/2} n)$ [2, 10, 1].

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